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DEC 27 2006

REMARKS

Claims 71-73, 76 and 78-81 remain pending in the application.

The pending claims stand rejected over Walker, Yamazaki-1, Yamazaki-2, Bulgaria, and Hsu.

Claims 71-73, 76 and 78-81 are believed allowable over the cited references for at least the reason that there is no prior art motivation to combine the references to create systems having the recited combinations of features of such claims.

Referring initially to claim 71, from which the remaining claims depend, such recites a computer system comprising an inverter which includes a structure comprising silicon and germanium; a PFET supported by the structure; an insulative material over at least a portion of the PFET; a first layer of semiconductive material over the insulative material; a second layer of semiconductive material over the first layer, with the second layer being compositionally different from the first layer; and an NFET over the insulative material and supported by the first and second layers of semiconductive material, with the NFET having a gate which is directly over a gate of the PFET.

The Examiner rejects claim 71 over Walker in combination with Yamazaki-1 and Yamazaki-2. Specifically, the Examiner cites Walker to show that it was known in the art to provide a computer system having an inverter which contains a pair of stacked transistor gates, and cites the Yamazaki references for teaching that transistor constructions can have paired semiconductive material layers over insulative material (Yamazaki-1), and that one of the paired semiconductive layers of Yamazaki-1 may comprise silicon-germanium (Yamazaki-2). In other words, the Examiner recognizes that Walker does not teach

stacked transistors having the claim 71 recited insulative material and first and second layers of semiconductive material between the stacked transistors. The Examiner looks to Yamazaki-1 for teaching that transistor structures can comprise gates over paired semiconductive material layers, and contends that it would be obvious to utilize the structures of Yamazaki-1 in the stacked construction of Walker. The Examiner contends that the motivation to combine Yamazaki-1 with Walker is that there can be a reduced nickel content in one of the semiconductive material layers of Yamazaki.

Applicant respectfully submits that there is no teaching within the Yamazaki references or Walker which would lead a person of ordinary skill in the art to combine the references to create a system of the type recited in claim 71. Substitution of the transistor structure of Yamazaki for one of the transistor structures of Walker would produce significant changes to the Walker structure, and render it inoperable for the purposes that Walker describes. Specifically, the transistor structures of Walker are non-volatile (specifically FLASH structures) utilized in a non-volatile memory array. In contrast, the transistor structure of Yamazaki is a thin film transistor that is not configured as non-volatile memory.

There is no teaching with Yamazaki that the transistor structures shown therein can be readily incorporated into FLASH configurations. Further, even if the structures of Yamazaki could be incorporated into FLASH configurations, such would add additional processing to the fabrication schemes of Walker, which would complicate such fabrication schemes. Semiconductor processing has a continuing goal of simplifying processing in order to increase throughput and reduce sources of error. Accordingly, it would not be

obvious to complicate the processing schemes of Walker by incorporating transistor structures of Yamazaki into the structures of Walker. Further, since there is no teaching within the references that the structures of Yamazaki are suitable for fabrication of non-volatile memory, and since Walker is directed toward fabrication of non-volatile memory, it would not be obvious to incorporate the structures of Yamazaki into the memory of Walker.

The Examiner's stated motivation for incorporating the teachings of Yamazaki's references into Walker is not appropriate motivation under §103. The Examiner's stated motivation is that Yamazaki has reduced nickel in one of the semiconductor layers taught therein. However, if the semiconductor layers of Yamazaki's references are not incorporated into Walker, the problem of nickel contamination never arises. In other words, the problems stated by the Examiner for supporting the combination of the Yamazaki references with Walker can be avoided by not combining Walker and the Yamazaki references in the first place. Thus, the Examiner's stated motivation for combining Walker and the Yamazaki references is almost circular reasoning. The motivation only makes sense if one has decided to combine the Yamazaki references and Walker in the first place. The motivation does not inspire the initial combination of Walker and the Yamazaki references, and if anything actually inspires not combining the Yamazaki references with Walker in order to avoid the problems of nickel contamination. For this additional reason, claim 71 is not rendered obvious by the combination of Walker with the Yamazaki references.

For the above-discussed reasons, claim 71 is allowable over the cited combination of Walker, Yamazaki-1 and Yamazki-2. It is noted that the Examiner's other cited

references do not provide any motivation or teachings which would inspire a person of ordinary skill in the art to combine the Yamazaki references with Walker. For the reasons presented herein, Applicant therefore respectfully requests allowance of claim 71 in the Examiner's next action.

Claims 72, 73, 76 and 78-81 depend from claim 71, and are therefore allowable for at least the reasons for which claim 71 is allowable.

Claims 71, 73, 76 and 78-81 are allowable over the cited references for the reasons discussed above, the applicant therefore requests formal allowance of such claims in the Examiner's next action.

Respectfully submitted

Dated: 12/27/06

By: _____

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